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ADVANCE INFORMATION

87C196CA/87C196CB 20 MHz ADVANCED 16-BIT CHMOS MICROCONTROLLER WITH INTEGRATED CAN 2.0

Automotive

- High Performance CHMOS 16-Bit CPU (up to 20 MHz Operation)
- Register-Register Architecture
- Up to 56 Kbytes of On-Chip EPROM
- Up to 1.5 Kbyte of On-Chip Register RAM
- Up to 512 Bytes of Additional RAM (Code RAM)
- Up to 16 Mbyte Linear Address Space
- Supports CAN (Controller Area Network) Specification 2.0
- 15 Message Objects of 8 Bytes Data Length
- 10-Bit A/D with Sample/Hold
- 38 Prioritized Interrupts
- Up to Seven 8-Bit (60) I/O Ports
- Full Duplex Serial Port (SIO) with Dedicated Baudrate Generator
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Interprocessor Communication Slave Port
- Selectable Bus Timing Modes for Flexible Interfacing
- Oscillator Fail Detection Circuitry
- High Speed Peripheral Transaction Server (PTS)
- Two Dedicated 16-Bit High-Speed Compare Registers
- High Speed Capture/Compare (EPA)
- Two Flexible 16-Bit Timer Counters
- Flexible 8-/16-Bit External Bus (Programmable)
- Programmable Bus (HLD/HLDA)
- 1.4 µs 16 x 16 Multiply
- 2.4 µs 32/16 Divide

−40°C to +125°C Ambient

Device	Pins/Package	EPROM	Reg RAM	Code RAM	I/O	EPA	SIO	SSIO	CAN	A/D	Address Space
87C196CB	84-Pin PLCC	56K	1.5K	512b	56	10	Y	Y	Y	8	1 Mbyte
87C196CB	100-Pin QFP	56K	1.5K	512b	60	10	Y	Y	Y	8	16 Mbyte
87C196CA	68-Pin PLCC	32K	1.0K	256b	38	6	Y	Y	Y	6	64 Kbyte

The 87C196CA/CB are new members of the MCS® 96 microcontroller family. These devices are based upon the MCS 96 Kx/Jx microcontroller product families with enhancements ideal for automotive and industrial applications. The CA/CB are the first devices in the Kx family to support networking through the integration of the CAN 2.0 (Controller Area Network) peripheral on-chip. The 87C196CB offers the highests memory density of the MCS 96 microcontroller family, with 56K of on-chip EPROM, 1.5K of on-chip register RAM, and 512 bytes of additional RAM (Code RAM). In addition, the 87C196CB provides up to 16 Mbyte of Linear Address Space. The 87C196CA is a sub-set of the CB, offering 32K of on-chip EPROM, up to 1.0K of on-chip register RAM, and 256 bytes of additional RAM (Code RAM).

April 1996 Order Number: 272405-004

The MCS 96 microcontroller family members are all high-performance microcontrollers with a 16-bit CPU. The 87C196CB is composed of the high-speed (20 MHz) macrocore with up to 16 Mbyte linear address space, 56 Kbytes of program EPROM, up to 1.5 Kbytes of register RAM, and up to 512 bytes of code RAM (16-bit addressing modes) with the ability to execute from this RAM space. It supports the high-speed, serial communications protocol CAN 2.0, with 15 message objects of 8 bytes data length, an 8-channel, 10-bit / 3 LSB analog to digital converter with programmable S/H times, and conversion times $< 20\ \mu s$ at 20 MHz. It has an asynchronous/synchronous serial I/O port (SIO) with a dedicated 16-bit baud rate generator, an additional synchronous serial I/O port (SSIO) with full duplex master/slave transceivers, a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities. There are ten modularized, multiplexed, high-speed I/O for capture and compare (called Event Processor Array) with 200 ns resolution and double buffered inputs, and a sophisticated prioritized interrupt structure with programmable Peripheral Transaction Server (PTS) implementing several channel modes, including single/burst block transfers from any memory location to any memory location, a PWM and PWM toggle mode to be used in conjunction with the EPA , and an A/D scan mode.

NOTICE:

This is an advance information data sheet. The A.C. and D.C. parameters contained within this data sheet may change after full automotive temperature characterization of the device has been performed. Contact your local sales office before finalizing the timing and D.C. characteristics of a design to verify you have the latest information.

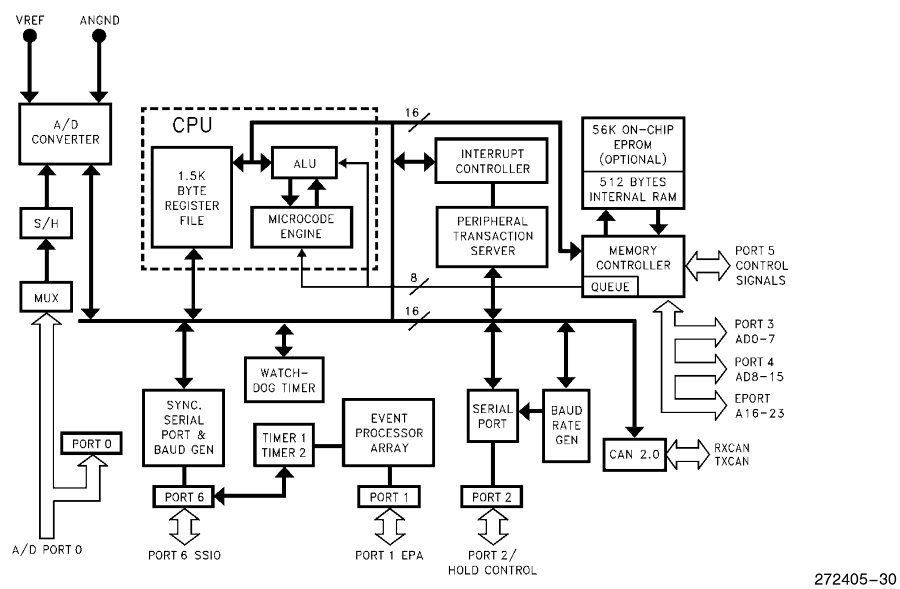


Figure 1. 8XC196CB Block Diagram

PROCESS INFORMATION

These devices are manufactured on P629.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

All thermal impedance data is approximate for static air conditions at 1.0W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

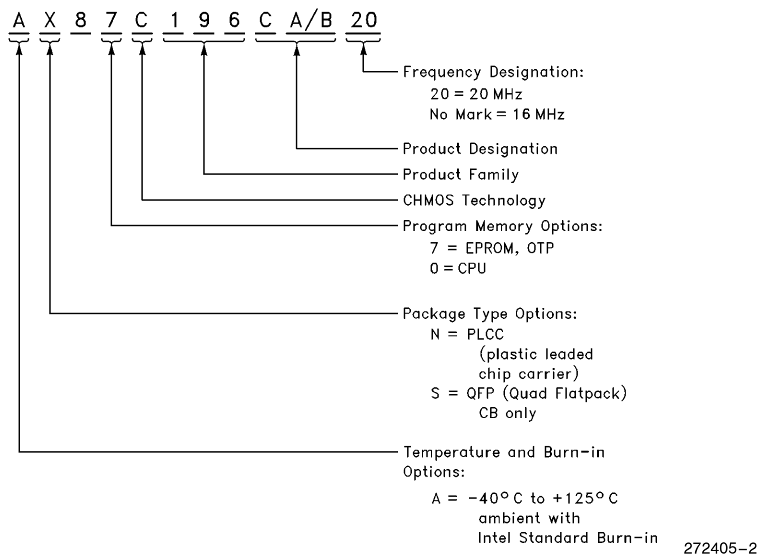


Figure 2. The 87C196CA/CB Familiy Nomenclature

Thermal Characteristics

Device and Package	θ_{JA}	θ_{JC}
AN87C196CB (84-Lead PLCC Package)	35.0°C/W	11.0°C/W
AN87C196CA (68-Lead PLCC Package)	36.5°C/W	10.0°C/W

NOTES:

1. θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient) measurements are taken 1 ft. away from case in air flow environment.
   θ_{JC} = Thermal resistance between junction and package face (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ±2°C/W.
3. Values listed are at a maximum power dissipation of 1.0W.

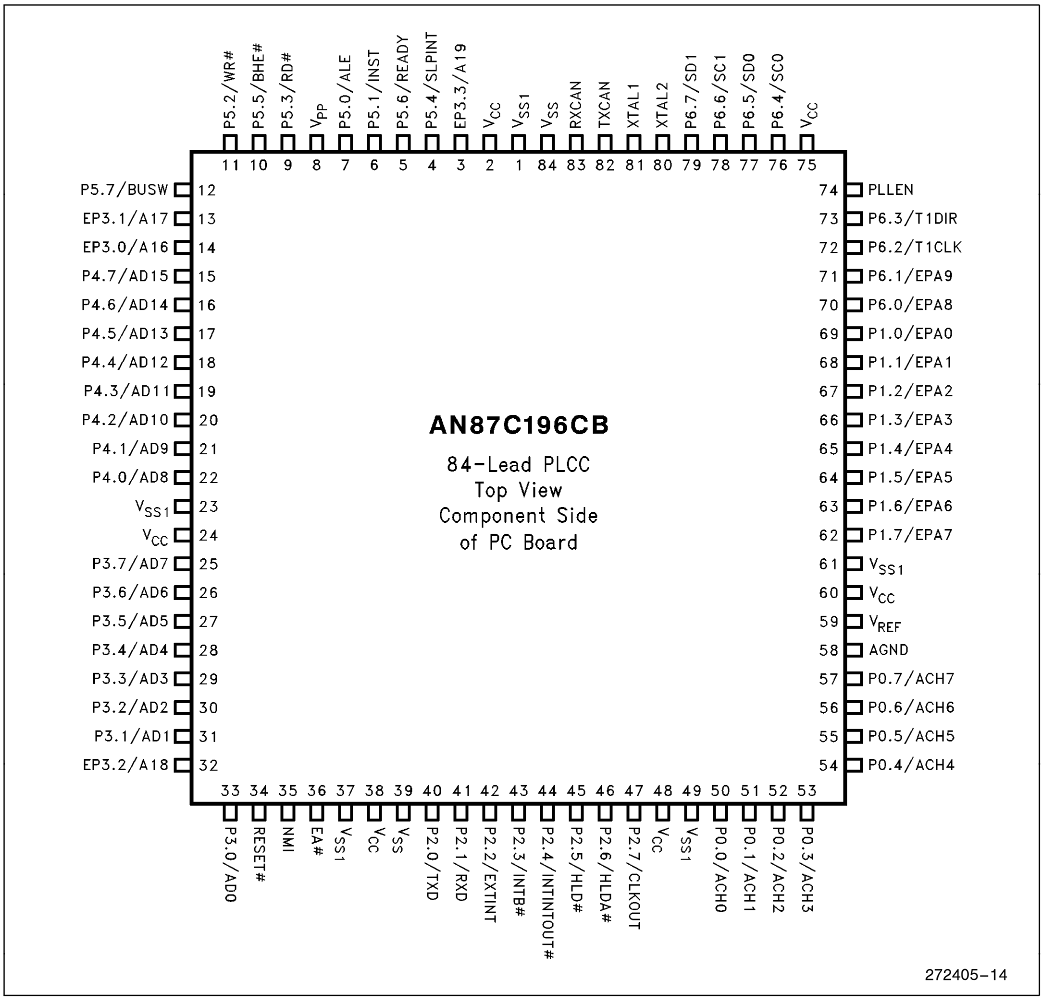


Figure 3. 84-Pin PLCC AN87C196CB Diagram

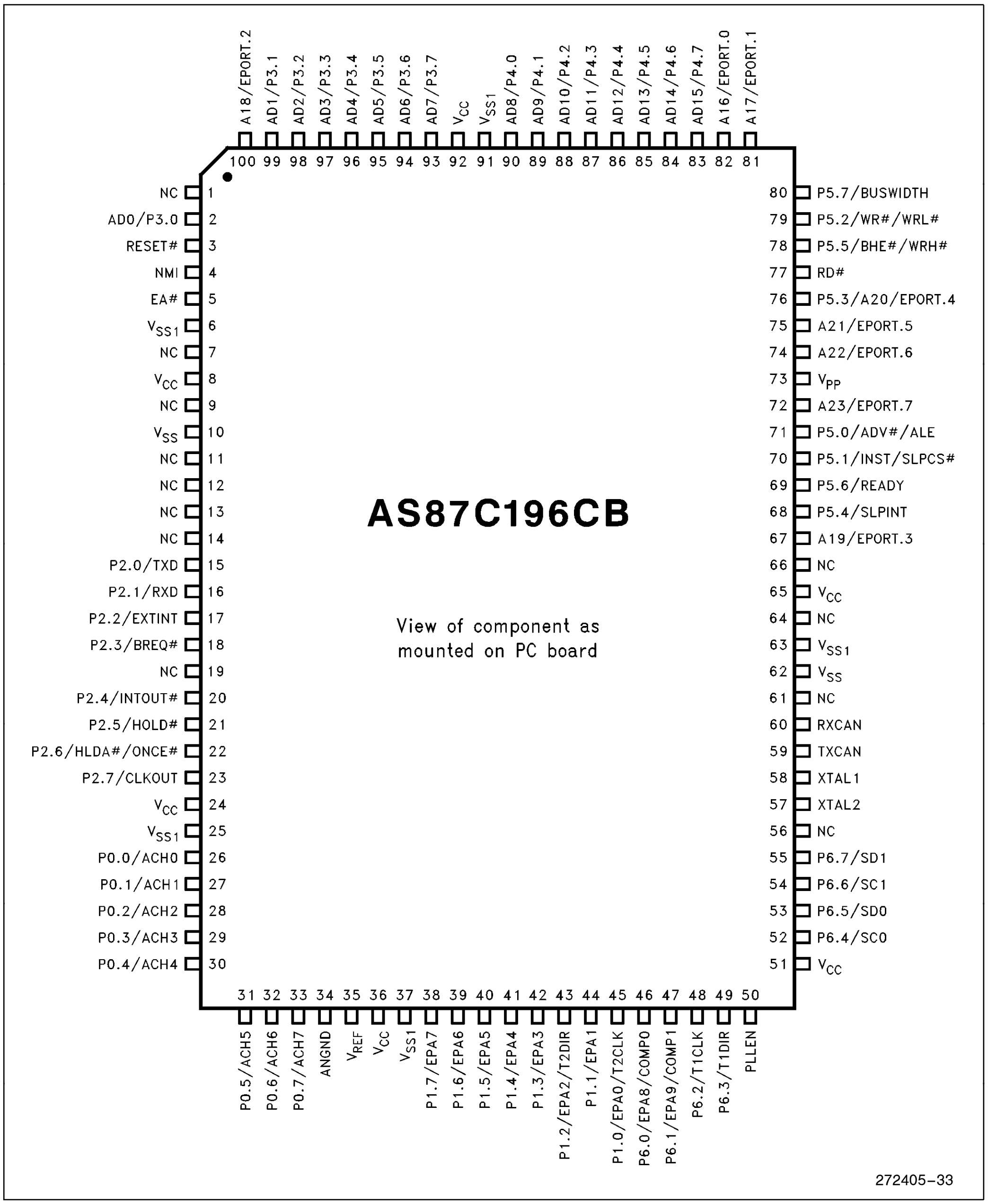


Figure 4. 100-Pin QFP AS87C196CB Diagram

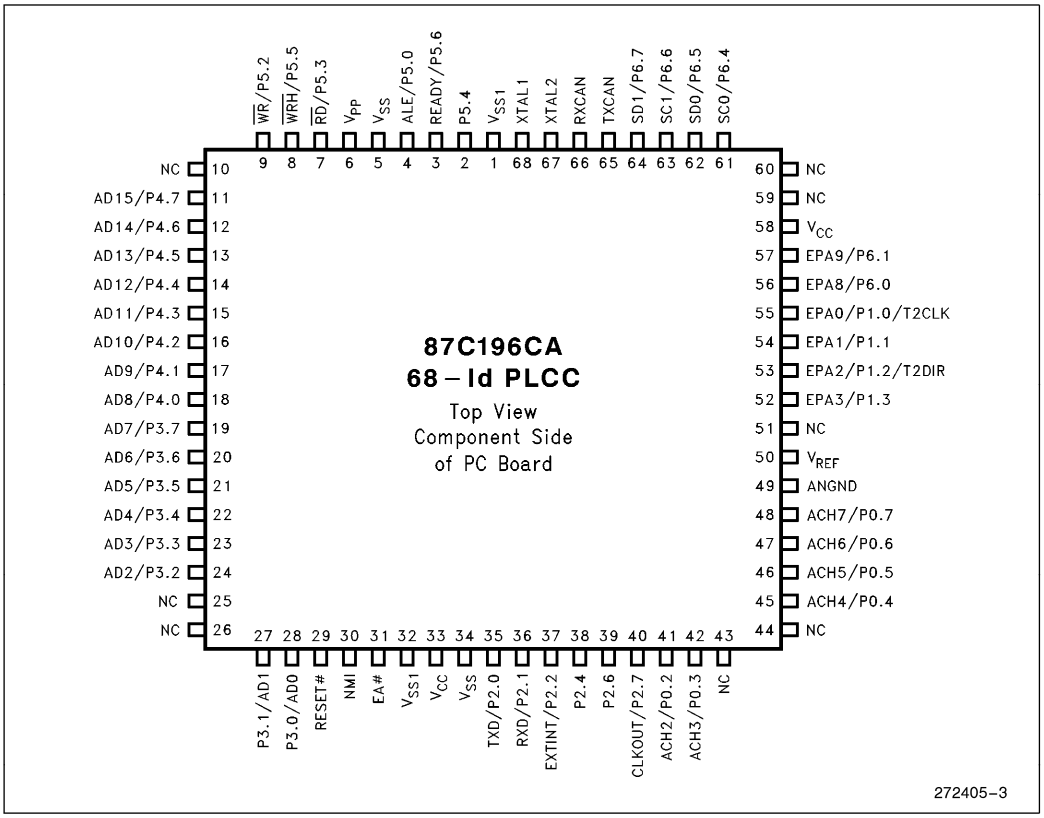


Figure 5. 68-Pin PLCC 87C196CA Diagram

Symbol	Name and Function
V_{CC}	Main Supply Voltage (+5V).
V_{SS},V_{SS1}	Digital circuit ground (0V). There are 7 V_{SS} pins CB (4 on CA), all of which MUST be connected to a single ground plane.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1Mohm resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the Oscillator Inverter.
RESET#	Reset input to the chip. Input low for at least 16 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, bytes are read from 2018H, 201Ah and 201CH (if enabled) loading the CCB's, and a jump to location 2080H is executed. Input high for normal operation. RESET# has an internal pullup.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
EA#	Input for memory select (External Access). EA# equal to a high causes memory accesses to locations 0FF2000H through 0FFFFFFH to be directed to on-chip EPROM/ROM. EA# equal to a low causes accesses to these locations to be directed to off-chip memory. EA# = +12.5V causes execution to begin in the Programming Mode. EA# is latched at reset.
PLLEN (196CB only)	Selects between PLL mode or PLL bypass mode. This pin must be either tied high or low. PLLEN pin = 0, bypass PLL mode. PLLEN pin = 1, places a 4x PLL at the input of the crystal oscillator. Allows for a low frequency crystal to drive the device (i.e., 5 MHz = 20 MHz operation).
P6.4–6.7/SSIO	Dual function I/O ports have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data providing for full duplex capability. Also LSIO when not used as SSIO.
P6.3/T1DIR (CB only)	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
P6.2/T1CLK (CB only)	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare.

Symbol	Name and Function
P5.7/BUSWIDTH (CB only)	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dynamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is "0" and CCR1 bit 2 is "1", all bus cycles are 8-bit, if CCR bit 1 is "1" and CCR1 bit 2 is "0", all bus cycles are 16-bit. CCR bit 1 = "0" and CCR1 bit 2 = "0" is illegal. Also an LSIO pin when not used as BUSWIDTH.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next opositive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/CCR1. Also an LSIO if READY is not selected.
P5.5/BHE#/WRH#	Byte High Enable or Write High output, as selected by the CCR. BHE# = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, BHE# = 1), to the high byte only (A0 = 1, BHE# =0) or both bytes (A0 = 0, BHE# = 0). If the WRH# function is selected, the pin will go low if the bus cycle is writing to an odd memory location. BHE#/WRH# is only valid during 16-bit external. Also an LSIO pin when not BHE/WRH#.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin (on CA, bidirectional port pin only).
P5.3/RD#	Read signal output to external memory. RD# is active only during external memory reads or LSIO when not used as RD#.
P5.2/WR#/WRL#	Write and Write Low output to external memory, as selected by the CCR, WR# will go low for every external write, while WRL# will go low only for external writes where an even byte is being written. WR#/WRL# is active during external memory writes. Also an LSIO pin when not used as WR#/WRL#.
P5.1/INST (CB only)	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM fetches INST is held low. Also LSIO when not INST.
P5.0/ALE/ADV#	Address Latch Enable or Address Valid Output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is ADV#, it goes inactive (high) at the end of the bus cycle. ADV# can be used as a chip select for external memory. ALE/ADV# is active only during external memory accesses. Also LSIO when not used as ALE.

Symbol	Name and Function
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is the oscillator frequency. CLKOUT has a 50% duty cycle. Also LSIO pin when not used as CLKOUT.
P2.6/HLDA#	Bus Hold Acknowledge. Active-low output indicates that the bus controller has relinquished control of the bus. Occurs in response to an external device asserting the HLD# signal. Also LSIO when not used as HLDA#.
P2.5/HLD# (CB only)	Bus Hold. Active-low signal indictes that an external device is requesting control of the bus. Also LSIO when not used as HLD#.
P2.4/INTOUT#	Interrupt Output. This active-low output indicates that a pending interrupt requires use of the external bus. Also LSIO when not used as INTOUT#
P2.3/BREQ# (CB only)	Bus Request. This active-low output signal is asserted during a HOLD cycle when the bus controller has a pending external memory cycle. Also LSIO when not used as BREQ#
P2.2/EXTINT	A positive transition on this pin causes a maskable interrupt vector through memory location 203CH. Also LSIO when not used as EXTINT.
P2.1/RXD	Receive data input pin for the Serial I/O port. Also LSIO if not used as RXD.
P2.0/TXD	Transmit data output pin for the Serial I/O port. Also LSIO if not used as TXD.
PORT 1/EPA0–7	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH0–7	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
EPORT (CB only)	8-bit bidirectional standard and I/O Port. These bits are shared with the extended address bus, A16–A19 for CB PLCC, A16–A23 for CB QFP. Pin function is selected on a per pin basis.
TXCAN	Push-pull output to the CAN bus line.
RXCAN	High impedance input-only from the CAN bus line.

87C196CB Memory Map

Address	Description
FFFFFFH FF2080H	Program Memory - Internal EPROM or External Memory (Determined by EA# Pin)
FF207FH FF2000H	Special Purpose Memory (Internal EPROM or External Memory) (Determined by EA# Pin)
FF1FFFH FF0600H	External Memory
FF05FFH FF0400H	Internal RAM (Identically Mapped into 00400H–005FFH)
FF03FFH FF0100H	External Memory
FF00FFH FF0000H	Reserved for ICE
FEFFFFH 0F0000H	Overlayed Memory (External)—Accesses into Memory Ranges 0F0000H to FEFFFFH will Overlay Page 15 (0FH) for CB QFP package—External Memory.(5)
0EFFFFH 010000H	900 Kbytes External Memory
00FFFFH 002080H	External Memory or Remapped OTPROM (Program Memory)(1)
00207FH 002000H	External Memory or Remapped OTPROM (Special Purpose Memory)(1, 3)
001FFFH 001FE0H	Memory Mapped Special Function Registers (SFR's)
001FDFH 001F00H	Internal Peripheral Special Function Registers (SFR's)(5)
001EFFH 001E00H	Internal CAN Peripheral Memory(5)
001DFFH 001C00H	Internal Register RAM
001BFFH 000600H	External Memory
0005FFH 000400H	Internal RAM (Code RAM) (Address with Indirect or Indexed Modes)
0003FFH 000100H	Register RAM – Upper Register File (Address with Indirect or Indexed Modes or through Windows.)(2)

87C196CB Memory Map (Continued)

Address	Description
0000FFH 000018H	Register RAM – Lower Register File. (Address with Direct, Indirect, or Indexed Modes.)(2)
000017H 000000H	CPU SFR's(4)

NOTES:
1. These areas are mapped internal EPROM if the REMAP bit (CCB2.2) is set and EA# = 5V. Otherwise they are external memory.
2. Code executed in locations 0000H to 003FFH will be forced external.
3. Reserved memory locations must contain 0FFH unless noted.
4. Reserved SFR bit locations must be written with 0.
5. Refer to 8XC196CB User's Guide for SFR, CAN and Paging Descriptions.

87C196CA Memory Map

Address	Description
00FFFFH 00A000H	External Memory
009FFFH 002080H	Internal EPROM (32 Kbytes)
00207FH 002000H	Reserved Memory (Internal EPROM or External Memory) (Determined by EA# Pin)
001FFFH 001FE0H	Memory Mapped Special Function Registers (SFR's)
001FDFH 001F00H	Internal Special Function Registers (SFR's)(1)
001EFFH 001E00H	Internal CAN Peripheral Memory
001DFFH 000500H	External Memory
0004FFH 000400H	Internal RAM (Code RAM) (Address with Indirect or Indexed Modes)
0003FFH 000100H	Internal Register RAM – Upper Register File (Address with Indirect or Indexed Modes or through Windows)(2)
0000FFH 000018H	Internal Register RAM – Lower Register File (Address with Direct, Indirect, or Indexed Modes(2).
000017H 000000H	CPU Special Function Registers (SFR's)(2, 4)

NOTES:
1. Refer to 8XC196KX Family User's Guide for SFR Description.
2. Code executed in locations 0000H to 03FFH will be forced external.
3. Reserved SFR bit locations must be written with 0.

CCB (2018h : Byte)

Bit	Field		Description
0	PD	=	"1" Enables Powerdown
1	BW0	=	See Table
2	WR	=	"1" = WR#/BHE—"0" = WRL#/WRH#
3	ALE	=	"1" = ALE—"0" = ADV#
4	IRC0	=	See Table
5	IRC1	=	See Table
6	LOC0	=	See Table
7	LOC1	=	See Table

CCB1 (201Ah : Byte)

Bit	Field		Description
0	CCR2	=	"1" fetch CCB2 ("0" for CA)
1	IRC2	=	See Table
2	BW1	=	See Table
3	WDE	=	"0" = Always Enabled
4	1	=	Reserved Must Be "1"
5	0	=	Reserved Must Be "0"
6	MEMSEL0	=	See Table ("1" for CA)
7	MEMSEL1	=	See Table ("1" for CA)

CCB2 (201Ch : Byte) (CB Only)

Bit	Field		Description
0	0	=	Reserved Must be "0"
1	MODE16	=	Select 16-Bit or 24-Bit Mode
2	REMAP	=	"0"—Select EPROM/CODERAM in Segment 0FFH only "1"—Select Both Segment 0FFH and Segment 00H
3	1	=	Reserved Must be "1"
4	1	=	Reserved Must be "1"
5	1	=	Reserved Must be "1"
6	1	=	Reserved Must be "1"
7	1	=	Reserved Must be "1"

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Write Protected Only
1	0	Read Protected Only
1	1	No Protection

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

MSEL1	MSEL0	"CB" Bus Timing Mode
0	0	Mode 0 (1-Wait KR)
0	1	Reserved Must Not Be Used
1	0	Reserved Must Not Be Used
1	1	Mode 3 (KR)

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BW Pin Controlled

Mode 0 (1-Wait KR): Designed to be similar to the 87C196KR bus timing with 1 automatic wait state.

See AC Timings section for actual timings data.

Mode 3 (KR): Designed to be similar to the 87C196KR bus timing.

See AC Timings section for actual timings data.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .... −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND .... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND .... −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation.......................... 1.0W

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

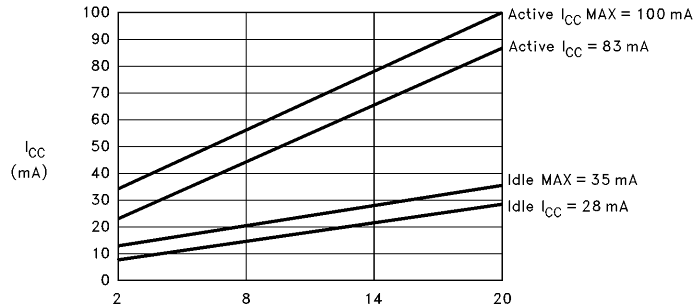
Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	20	MHz(4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

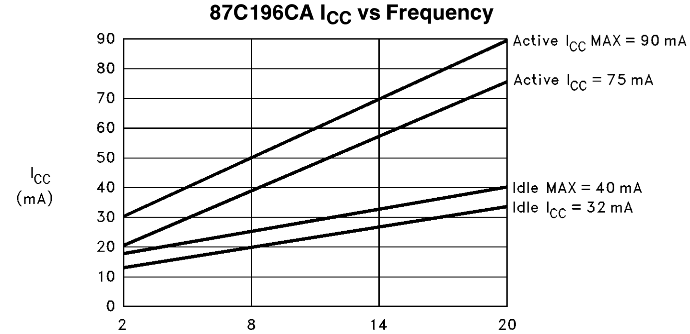
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	V_{CC} Supply Current (−40°C to +125°C Ambient) CA CB	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While device in Reset)			 90 100	 mA mA
I_{REF}	A/D Reference Supply Current				5	mA
I_{IDLE}	Idle Mode Current CA CB	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$			 40 35	 mA mA
I_{PD}	Powerdown Mode Current	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(6, 9)		50	TBD	μA
V_{IL}	Input Low Voltage (all pins)	For PORT0(8)	−0.5V		0.3 V_{CC}	V
V_{IH}	Input High Voltage	For PORT0(8)	0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)	I_{OL} = 200 μA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA			0.3 0.45 1.5	V V V
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	I_{OH} = −200μA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V

87C196CB I_{CC} vs Frequency



272405–31

87C196CA I_{CC} vs Frequency



272405–32

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current (Std. Inputs)	$V_{SS} < V_{IN} < V_{CC}$			±10	μA
I_{LI1}	Input Leakage Current (Port 0)	$V_{SS} < V_{IN} < V_{REF}$			CA ±1.5 CB ±1.0	μA
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	$I_{OH} = 0.8$ mA(7)	2.0			V
V_{OH2}	Output High Voltage in RESET	$I_{OH} = -15$ μA(1)	$V_{CC} - 1V$			V
C_S	Pin Capacitance (Any pin to V_{SS})	$f_{test} = 1.0$ MHz(6)			10	pF
R_{WPU}	Weak Pullup Resistance	(Note 6)		150K		Ω
R_{RST}	Reset Pullup Resistor	For CB	65K		180K	Ω
R_{RST}	Reset Pullup Resistor CA	For CA	6K		65K	Ω

NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5 and Port6 except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
9. For temperatures <100°C typical is 10 μA.

8XC196CB ADDITIONAL BUS TIMING MODES

The 8XC196CB device has 2 bus timing modes for external memory interfacing.

MODE 3:

Mode 3 is the standard timing mode. Use this mode for systems that emulate the 8XC196KR bus timings.

MODE 0:

Mode 0 is the standard timing mode, but 1 (minimum) wait state is always inserted in external bus cycles.

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196CA/CB will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50.0	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	μs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns
T_{CLLH}	CLKOUT Low to ALE/ADV High	−15	+10	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	−20	+15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	T_{OSC} − 30		ns
T_{RLCL}	RD Low to CLKOUT Low CA CB	 +4 −8	 +30 +20	 ns ns
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 10		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	−5	+25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period CB CA	 T_{OSC} − 30 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{OSC} − 25		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ High	T_{OSC} − 10		ns
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 Tosc × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. Programming the CDE bit enables oscillator fail detection.

AC CHARACTERISTICS (Over Specified Operating Conditions)

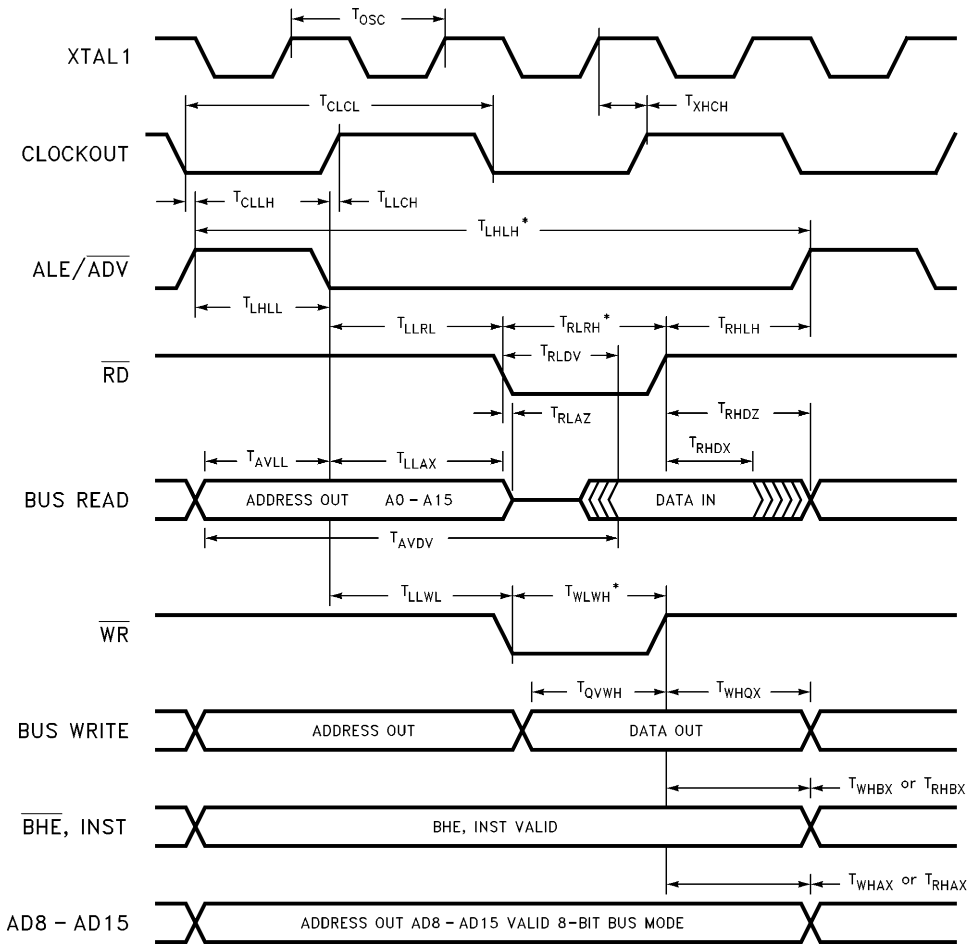
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise anf Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196CA/CB.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\ T_{OSC} - 75$	ns(3)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\ T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\ T_{OSC} - 55$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid CA CB		 $T_{OSC} - 22$ $T_{OSC} - 30$	 ns(2) ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 Tosc × n, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

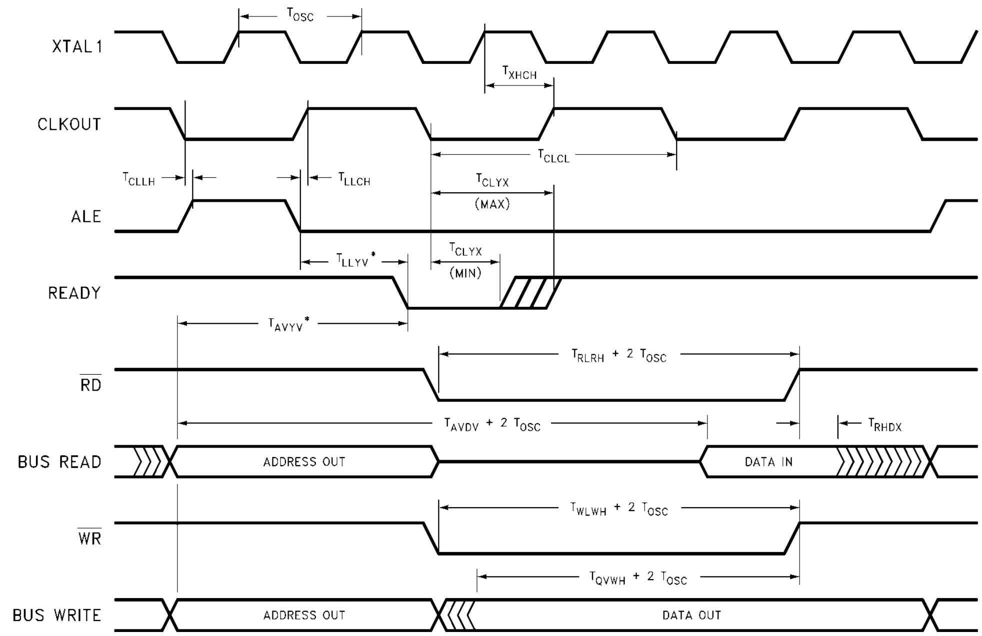
87C196CA/CB SYSTEM BUS TIMING



272405–17

* If mode 0 operation is selected, add 2 Tosc to this time.

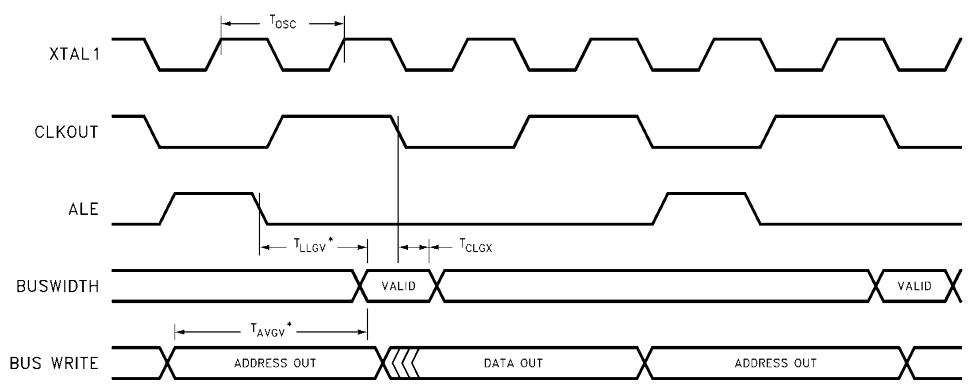
87C196CA/CB READY TIMINGS (ONE WAIT STATE)



272405–18

*If mode 0 selected (CB only), one wait state is always added. If additional wait states are required, add 2 Tosc to these specifications.

87C196CB BUSWIDTH TIMINGS



272405–19

*If mode 0 selected (CB only), add 2 Tosc to these specifications.

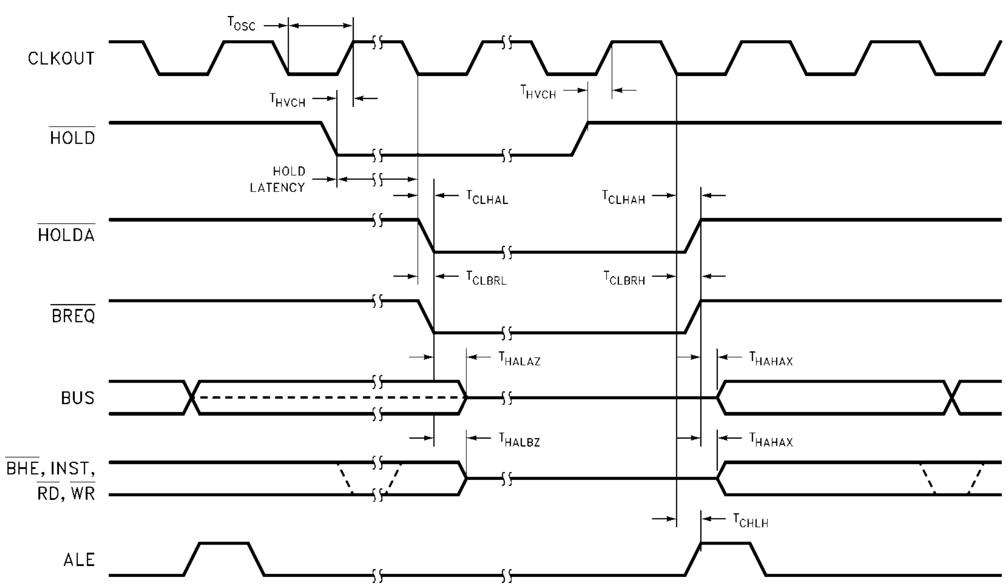
8XC196CB HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	+15	ns
T_{AZHAL}	HLDA Low to Address Float		+20	ns
T_{BZHAL}	HLDA Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	−15	+15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	−25	+25	ns
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns
T_{HAHBV}	HLDA High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10	+15	ns

NOTE:
1. To guarantee recognition at next clock.

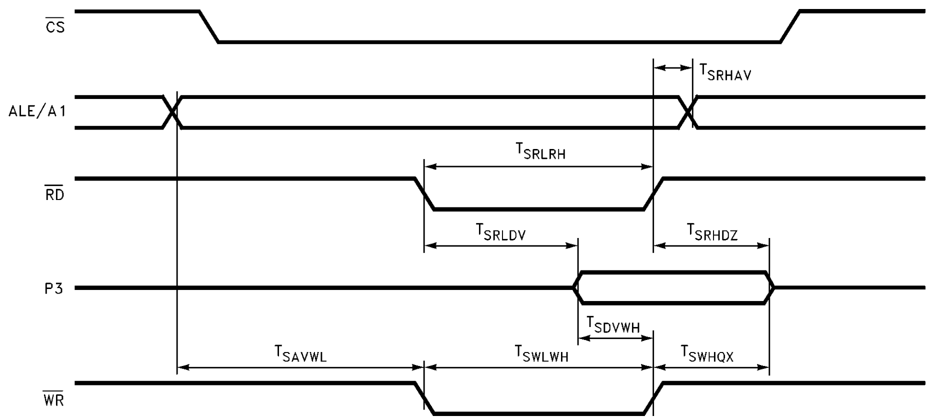
8XC196CB $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



272405–20

8XC196CB AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



272405–21

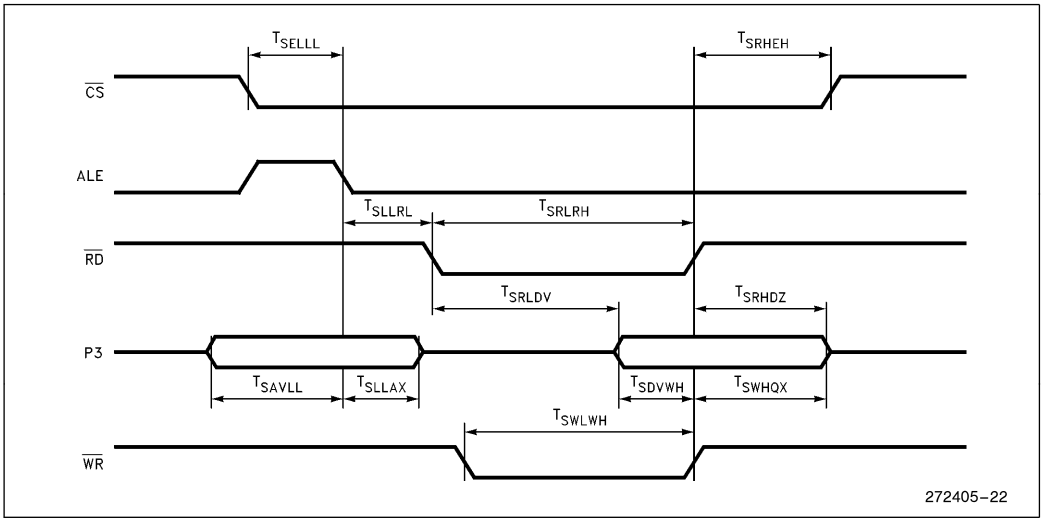
SLAVE PORT TIMING—(SLPL = 0, 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

t = 1 state time (125 ns @ 16 MHz)

NORMAL MASTER/SLAVE OPERATION

Symbol	Parameter	Min	Max	Units
T_{CHCH}	Clock Period	4t		ns
T_{CLCH}	Clock Low Time/Clock High Time	2t −10		ns(1)
T_{CLDV}	Clock Falling to Data Out Valid (Master)	0.5t	1.5t + 20	ns
T_{CLDV1}	Clock Falling to Data Out Valid (Slave)	0.5t	1.5t + 50	ns
T_{DVCH}	Data In Setup to Clock Rising Edge	10		ns
T_{CHDX}	Clock Rising Edge to Data in Invalid	t + 15		ns

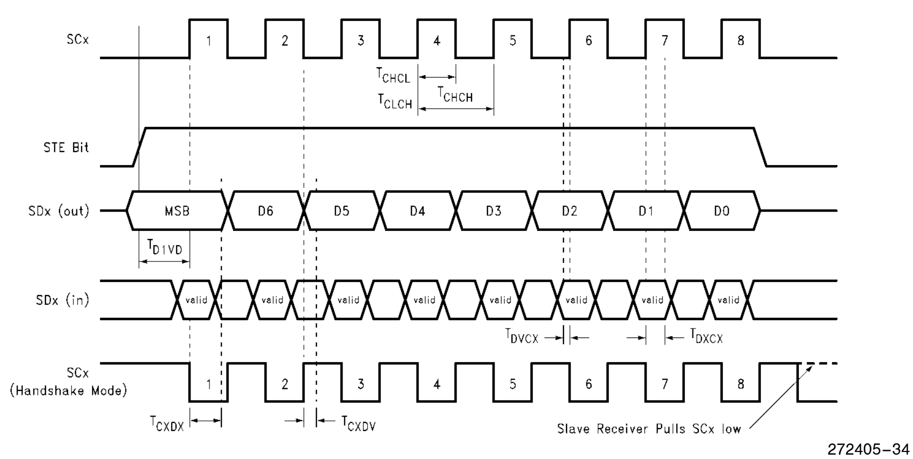
*Timings are guaranteed by design.

HANDSHAKE OPERATION

Symbol	Parameter	Min	Max	Units
T_{CHCH}	Clock Period	4t		ns
T_{CLCH}	Clock Low Time/Clock High Time	2t −10		ns(1)
T_{CLDV}	Clock Falling to Data Out Valid (Master)	0.5t	1.5t + 20	ns
T_{CLDV1}	Clock Falling to Data Out Valid (Slave)	0.5t	1.5t + 50	ns
T_{DVCH}	Data In Setup to Clock Rising Edge	10		ns
T_{CLDX}	Clock Rising Edge to Data in Invalid	t + 15		ns

*Timings are guaranteed by design.

NOTE:
1. This specification refers to input clocks during slave operation. During master operation, the device will output a nominal 50% duty cycle clock.



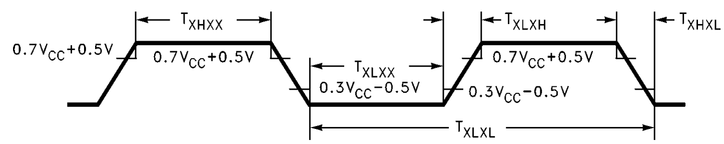
NOTE:
The top SCx signal assumes that the SSIO is configured to sample on the leading edge with an active-high clock signal. The SCx signal will be different for other configurations, however, setup and hold timings will still be the same in relation to the latching edge of SCx.

Figure 6. Synchronous Serial Port

EXTERNAL CLOCK DRIVE

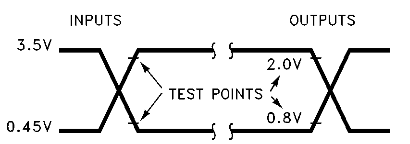
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	20	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	50.0	250	ns
T_{XHXX}	High Time	$0.35 \times T_{OSC}$	$0.65\ T_{OSC}$	ns
T_{XLXX}	Low Time	$0.35 \times T_{OSC}$	$0.65\ T_{OSC}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



272405–23

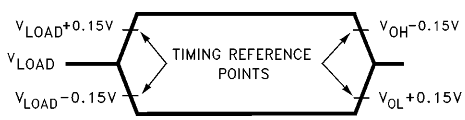
AC TESTING INPUT, OUTPUT WAVEFORMS



272405–24

AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



272405–25

For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:	Signals:	
H—High	A—Address	HA—$\overline{\text{HLDA}}$
L—Low	B—$\overline{\text{BHE}}$	L—ALE/$\overline{\text{ADV}}$
V—Valid	BR—$\overline{\text{BREQ}}$	Q—Data Out
X—No Longer Valid	C—CLKOUT	RD—$\overline{\text{RD}}$
Z—Floating	D—DATA	W—$\overline{\text{WR}}$/$\overline{\text{WRH}}$/$\overline{\text{WRl}}$
	G—Buswidth	X—XTAL1
	H—$\overline{\text{HOLD}}$	Y—READY

EPROM SPECIFICATIONS

AC EPROM PROGRAMMING CHARACTERISTICS

Operating Conditions: Load Capacitance = 150 pF; T_C = 25°C ±5°C, V_{CC}, V_{REF} = 5.0V ±0.5V, V_{SS}, ANGND = 0V.
V_{PP} = 12.5V ±0.25V; $\overline{EA}$ = 12.5V ± 0.25V; Fosc = 5.0 MHz.

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2) CA CB	 50 100		 T_{OSC} T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid CA CB		 50 100	 T_{OSC} T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with Fosc = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. Programming specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use 300 Tosc + 100 μs.

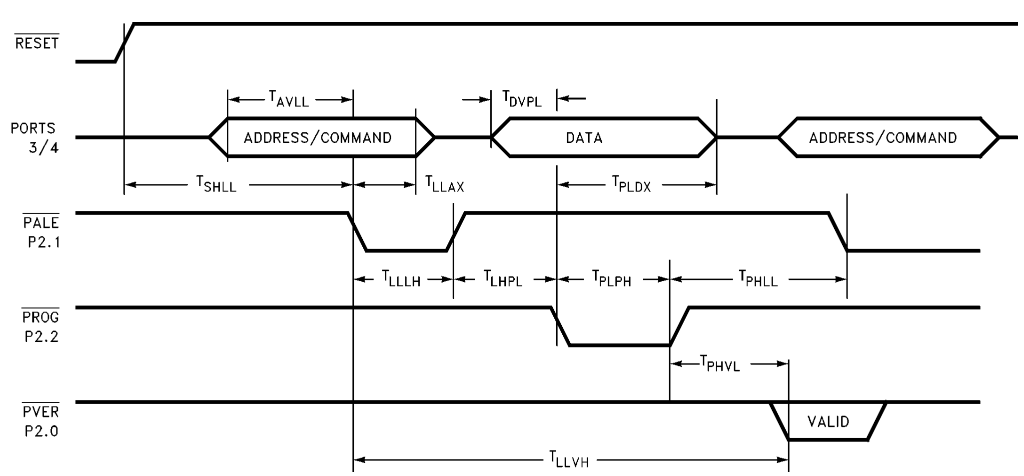
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5V.

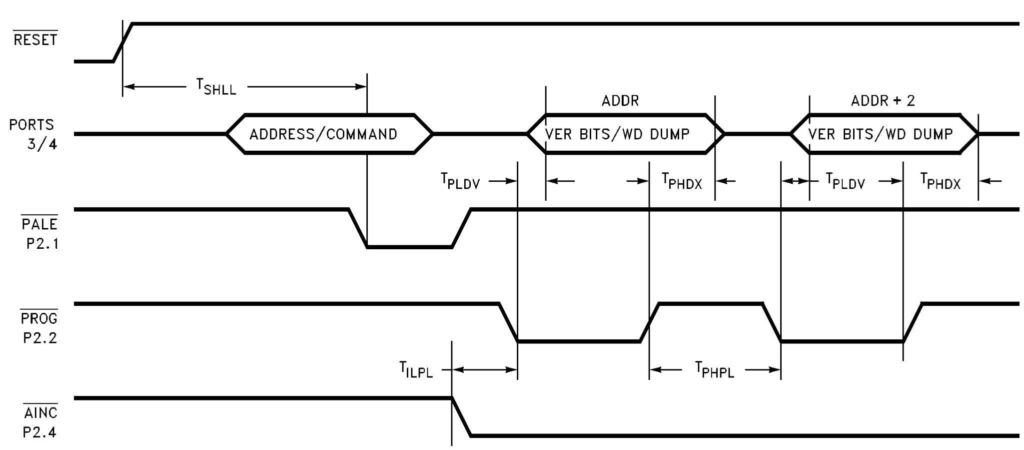
EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



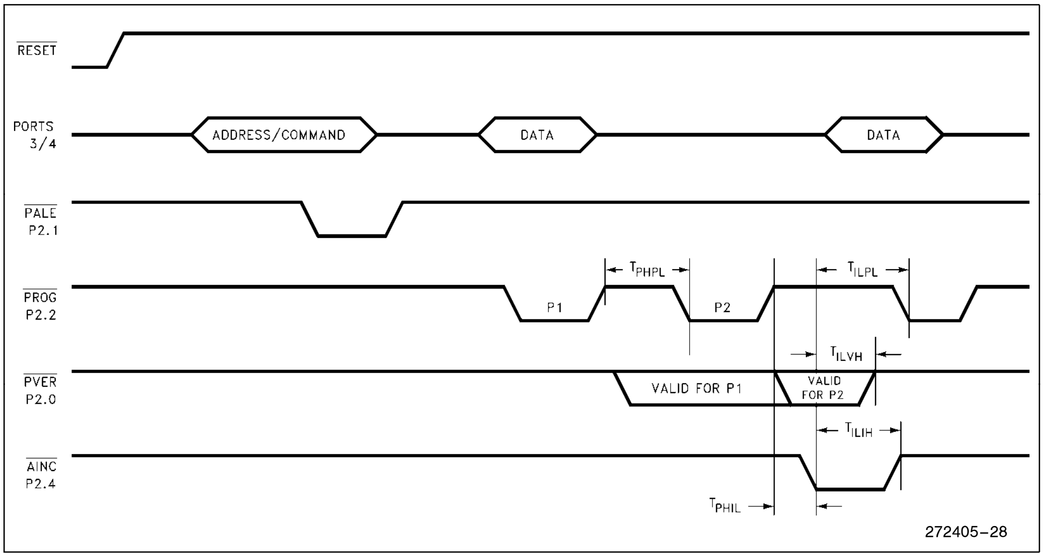
272405–26

SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



272405–27

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE 0

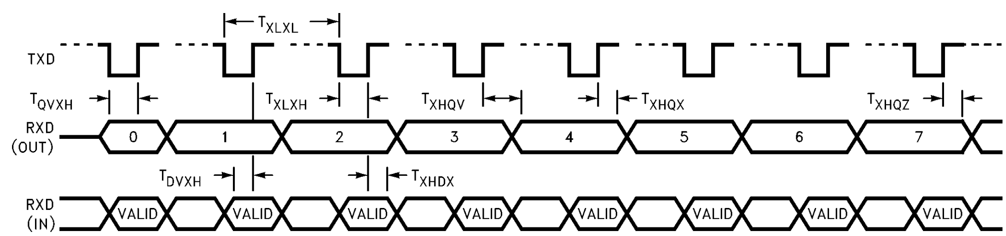
Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(8)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(8)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTE:
8. Parameters not tested.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



272405–29

A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specified in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, SAMP. The value loaded into AD_TIME bits 0, 1, 2, 3 and 4 determines the bit conversion time, CONV. These bits, as well as the equation for calculating the total conversion time, T, are shown in the following table:

AD_TIME 1FAFH:Byte

7	6	5	4	3	2	1	0
Sample Time			Bit Conversion Time				
(SAMP) 4n + 1 state times n = 1 to 7			(CONV) n + 1 state times n = 2 to 31				

Equation: $T = (SAMP) + Bx\,(CONV) + 2.5$
T = total conversion time (states)
B = number of bits conversion (8 or 10)
n = programmed register value

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is without doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 20 MHz operating frequency. After a conversion is started, the device is placed in IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	2.0		μs(2)
T_{CONV}	Conversion Time	15	18	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	2.0		μs(2)
T_{CONV}	Conversion Time	12	15	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±1.5	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

87C196CA DESIGN CONSIDERATIONS

The 87C196CA device is a memory scalar of the 87C196KR device with integrated CAN 2.0. The CA is designed for strict functional and electrical compatibility to the Kx family as well as integration of on-chip networking capability. The 87C196CA has fewer peripheral functions than the 196KR, due in part to the integration of the CAN peripheral. Following are the functionality differences between the 196KR and 196CA devices.

196KR Features Unsupported on the 196CA:
- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT and SLPCS Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer 1
- Quadrature Clocking Timer 1
- Dynamic Buswidth
- EPA Capture Channels 4–7

(1) **External Memory.** Removal of the Buswidth pin means the bus cannot dynamically switch from 8- to 16-bit bus mode or vice versa. The programmer must define the bus mode by setting the associated bits in the CCB.

(2) **Auto-Programming Mode.** The 87C196CA device will ONLY support the 16-bit zero wait state bus during auto-programming.

(3) **EPA4 through EPA7.** Since the CA device is based on the KR design, these functions are in the device, however there are no associated pins. A programmer can use these as compare-only channels or for other functions like software timer, start an A/D conversion, or reset timers.

(4) **Slave Port Support.** The Slave port can not be used on the 196CA due to a function change for P5.4/SLPINT and P5.1/SLPCS not being bonded-out.

(5) **Port Functions.** Some port pins have been removed. P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The PxREG, PxSSEL, and PxIO registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

Additionally, these port pins should be setup internally by software as follows:

1. Written to PxREG as "1" or "0".
2. Configured as Push/Pull, PxIO as "0".
3. Configured as LSIO.

This configuration will effectively strap the pin either high or low. *DO NOT Configure as Open Drain output "1", or as an Input pin. This device is CMOS.*

(6) **EPA Timer RESET/Write Conflict.** If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

(7) **Valid Time Matches.** The timer must increment/decrement to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

(8) **Write Cycle during Reset.** If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

(9) **Indirect Shift Instruction.** The upper 3 bits of the byte register holding the shift count are not masked completely. If the shift count register has the value $32 \times n$, where $n = 1, 3, 5,$ or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

(10) **P2.7 (CLKOUT).** P2.7 (CLKOUT) does not operate in open drain mode.

87C196CA ERRATA

This data sheet was published prior to first available silicon. Consequently, there is no known errata at this time.

87C196CA DESIGN CONSIDERATIONS

1. PORT0

On the 87C196CA the analog inputs for P0.0 and P0.1 have been multiplexed and tied to V_{REF}. Therefore, initiating an analog conversion on ACH0 or ACH1 will result in a value equal to full scale (3FFh). On the CA, the digital inputs for these two channels are tied to ground, therefore, reading P0.0 or P0.1 will result in a digital "0".

2. PORT1

On the 87C196CA, P1.4, P1.5, P1.6 and P1.7 have been removed from the device and is unavailable to the programmer. Corresponding bits in the port registers have been "hard-wired" to provide the following results when read:

Register Bits		When Read
P1_PIN.x	(x = 4,5,6,7)	1
P1_REG.x	(x = 4,5,6,7)	1
P1_DIR.x	(x = 4,5,6,7)	1
P1_MODE.x	(x = 4,5,6,7)	0

Writing to these bits will have no effect.

3. PORT2

On the 87C196CA, P2.3 and P2.5 have been removed from the device and are not available to the programmer. Corresponding bits in the port registers have been "hard-wired" to provide the following results when read.

Register Bits		When Read
P2_PIN.x	(x = 3,5)	1
P2_REG.x	(x = 3,5)	1
P2_DIR.x	(x = 3,5)	1
P2_MODE.x	(x = 3,5)	0

Writing to these bits will have no effect.

4. PORT5

On the 87C196CA, P5.1 and P5.7 have been removed from the device and are not available to the programmer. Corresponding bits in the port registers have been "hard-wired" to provide the following results when read:

Register Bits		When Read
P5_PIN.x	(x = 1,7)	1
P5_REG.x	(x = 1,7)	1
P5_DIR.x	(x = 1,7)	1
P5_MODE.x	(x = 1)	0
P5_MODE.x	(x = 7)	1

Writing to these bits will have no effect.

5. PORT6

On the 87C196CA, P6.2 and P6.3 have been removed from the device and are not available to the programmer. Corresponding bits in the port registers have been "hard-wired" to provide the following results when read:

Register Bits		When Read
P6_PIN.x	(x = 2,3)	1
P6_REG.x	(x = 2,3)	1
P6_DIR.x	(x = 2,3)	1
P6_MODE.x	(x = 2,3)	0

Writing to these bits will have no effect.

DATA SHEET REVISION HISTORY

This is the -003 revision of the 87C196CA/CB data sheet. The following differences exist between the -002 version and the -003 revision.

1. The data sheet has been revised to ADVANCE from PRELIMINARY, indicaitng the specifications have been verified through electrical tests.
2. The 87C196CB 100-ld QFP package and device pinout has been added to the data sheet.
3. The 87C196CB 100-ld QFP device supports up the 16 Mbyte of linear address space.
4. The package thermal characteristics for the PLCC packages was added to the data sheet, for the CB θ_{JA} = 35.0°C/W, θ_{JC} = 11.0°C/W. For the CA, θ_{JA} = 36.5°C/W and θ_{JA} = 10.0°C/W.
5. The AN87C196CB pin package diagram was corrected to show EA# as opposed to EA.
6. The REMAP bit funciton for CCB2 was corrected. Setting this bit to 0 selects EPROM/CODERAM in segment 0FFH only. Setting this bit to 1 selects both segment 0FFH and segment 00H.
7. t_{RLAZ} has been changed to 5 ns from 20 ns.
8. t_{WLWH} for the CA has been changed to t_{OSC} −20 from t_{OSC} − 30.
9. t_{CLGX} has been changed to 0 ns min, from t_{OSC} − 46 max.
10. Timing specifications for the SSIO are now added. These timings are currently guaranteed by design.
11. Added frequency designation to family nomenclature Figure 2.

This is the -002 revision of the 87C196CA data sheet. The following difference exist between the -001 version and the -002 revision.

1. This data sheet now includes the specifications for the 87C196CB as well as the 87C196CA.
2. ABSOLUTE MAXIMUM RATINGS have been added.
3. Maximum Frequency has been increased to 20 MHz.
4. Maximum ICC has been increased from 75 mA to 100 mA for the CB, 90 mA for the CA.
5. Idle Mode current has been increased to 35 mA from 30 mA for the CB, 40 mA for the CA.
6. Input leakage current for Port 0 (ILI1) was decreased to 1.5 μA from 2.0 μA for the CA.
7. The electrical characteristics for the CAN module were removed. The electrical characteristics for TXCAN and RXCAN are identical to standard port pins.
8. t_{OSC} (1/freq) was modified to reflect 20 Mhz timings.
9. t_{OFD} (Oscillator Fail Detect Specification) for clock failure to RESET pin pulled low, was added to the data sheet (4 μs min, 40 μs max)
10. t_{WHQX} has been increased to t_{OSC} − 25 ns min from t_{OSC} − 30 ns min.
11. t_{RXDX} has been replaced by t_{RHDX}. t_{RLAZ} has been increased to 20 ns max from 5 ns max.
12. I_{PP} programming supply current has been increased to 200 mA from 100 mA.
13. t_{CONV} Conversion time for 10 bit A/D conversions has been decreased to reflect 20 Mhz operation.
14. R_{RST} was added for the 87C196CA (min = 6 kΩ/max = 65 kΩ.
15. t_{CLLH}—min/max parameters switched to accurately reflect this timing parameter.
16. t_{RLCL}—Separate timings for the 87C196CA vs 87C196CB. t_{RLCL} for the CB is min −8 ns, max +20 ns. For the CA, t_{RLCL} min +4 ns/max +30 ns.
17. t_{RLRH} changed to T_{OSC} − 10 ns from T_{OSC} − 5 ns.
18. t_{AVGV} added for the 87C196CB.
19. t_{LLGV} added for the 87C196CB.
20. t_{CLGX} added for the 87C196CB.
21. t_{RLDV}—Separate timings for 87C196CB. t_{RLDV} max = T_{OSC} − 30 ns. For the 87C196CA, t_{RLDV} max = T_{OSC} − 22 ns.
22. HOLD/HOLDA timings added for the 87C196CB.
23. Slave Port Timings added for the 87C196CB.
24. Separate specifications for t_{PLPH} for the 87C196CB, t_{PLPH}, min = 100 T_{OSC}. For the 87C196CA, t_{PLPH} min = 50 T_{OSC}.
25. Separate specificatons for t_{PLDV} for the 87C196CB, t_{PLDV} min = 100 T_{OSC} for the 87C196CA, t_{PLDV} min = 50 T_{OSC}.
26. 8-Bit mode A/D characteristics added.